Sibo Zhang

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Education

University of Washington **Sep. 2023 – June 2027**
Bachelor of Science in Electrical and Computer Engineering | Dean's List | GPA: 3.71 *Seattle, WA*

Relevant Coursework

- Circuit Analysis
- Digital Circuits
- Semiconductor Devices
- Data Structure
- VLSI I/II
- Computer Architecture
- Machine Learning

Experience

Electrical and Computer Engineering, University of Washington **June 2025 – Present**
Teaching Assistant for VLSI I (EE 476) *Seattle, WA*

- Working with Professor Richard Shi to prepare materials for the course, including lectures, assignments, and labs
- Teaching students how to use Linux, Cadence Virtuoso, and HSPICE to analyze circuit schematics and layouts
- Instructing students about the fundamentals of VLSI, such as MOSFET behavior, RC delay, power, timing, and memory

PNCEL Lab, University of Washington **June 2025 – Present**
Research Assistant *Seattle, WA*

- Developing a CGRA-based CUDA-compatible energy-efficient alternative for GPGPUs
- Writing RTL code for the underlying structure of the CGRA GPU
- Running performance tests (simx and rtlsim) using various numbers of clusters, cores, warps, and threads
- Using CACTI to model and analyze cache memory performance (access time, power, cycle time, and area)

iMatter Lab, University of Washington **September 2024 – Present**
Research Assistant *Seattle, WA*

- Creating flexible 3D-printed thermoelectric generators producing 15 $\mu W/cm^2$ using bismuth telluride and eutectic gallium-indium (EGaIn)
- TEGs weigh 25 grams and are cost-efficient at just $15 per unit, suitable for scalable and wearable energy solutions
- Designing and creating flexible temperature and humidity sensors for real-world applications

Hu Lab, University of Illinois Urbana-Champaign **July 2024 – September 2024**
Research Assistant *Champaign, IL*

- Reduce buffering when streaming videos for applications such as YouTube and TikTok
- Used Linux and FFProbe to extract and analyze data from videos, such as frames and the presentation time stamp, and the size of packets
- Developed a Python program to sort out never-buffer strategy, bandwidth requirements, and RTT

Projects

16x13 Register File | *Cadence Virtuoso, HSPICE* **March 2025**

- Worked in a team of three to develop the schematic and layout for the register file
- Design consists of a 4-to-16 decoder, 16×13 array of DFFs, and a per-bit 16:1 read multiplexer network
- Used HSPICE to test the functionality and performance of the register file layout
- **Results:** Total area of 3,583.49 μm^2, clock frequency of 2.7 GHz, read energy of 9.972 pJ, and write energy of 13.03 pJ

ARM-based 5 Stage Pipeline CPU | *SystemVerilog, ModelSim* **November 2025**

- Designed and implemented an ARM-based 5-stage pipelined CPU in SystemVerilog
- Built a pipelined datapath with EX/MEM and MEM/WB data forwarding to resolve data and control hazards
- Verified functionality using custom testbenches and simulation

Snakes and Apples | *SystemVerilog, ModelSim, DE1-SoC* **March 2025**

- Imitate the game "Snake" and allow the user to play the game on hardware
- Hardware features include: DE1-SoC board, 16x16 LED expansion board, and external PS2 keyboard
- Software features include: increasing snake length, random apple generation, victory, and collision detection
- Debugged using ModelSim and the DE1-SoC board

Technical Skills

Programming Languages: Python, Java, SystemVerilog, HTML, CSS
Development Tools: Visual Studio Code, IntelliJ, GitHub, Quartus
Tools: Cadence Virtuoso, HSPICE, Linux, ModelSim, KiCAD, FFmpeg
Libraries: NumPy, Matplotlib, Pandas